Screen Display Module

This module contains all the routines necessary to input data to the user screen. This includes setting up the main user screen (task(iv)), and all the other screens during the various test modes. In the waterfall mode, this module displays the received characters from the DSP continuously on the screen - eighty characters every second (task (xiii). It also displays the current value of **baud_offset** as echoed by the DSP (task(xiv)). In the tune receiver mode, it again displays the value of **baud_offset**, and SER calculations (task (xviii)). In the SER calculation mode, the module only displays the results of the SER calculations. In the timed data collection mode, it only displays the task being done - either writing to RAM or writing to hard disk.

SER Module

This module is used by the application control module to perform symbol error calculations, keep a track of frame slips and bad symbols in the tune receiver and SER calculation modes (task (xviii)). For symbol error rate calculations to be performed a frame delimiter character is necessary in the transmitted signal. This frame delimiter character is available in the NWN.CNF file which the application module reads at the beginning of a test. Similarly the entire expected frame is also read when the test is set up. This information is then available for the SER module to use.

The calculations are performed on a per frame basis after the expected delimiter character. If a delimiter character is not detected, the entire frame prior to the expected delimiter character is discarded, and no symbol error calculations are performed. In terms of performance, this is recorded as a frame slip. As a result, information about bad symbols within a slipped frame are not available to the user. When a frame delimiter character is detected, the just received frame prior to the delimiter character is compared with the expected frame, and the number of bad symbols is recorded. A running sum of bad symbols, frame slips and total number of symbols received is maintained by this module, and passed to the screen routines periodically for display. If n is the running sum of symbols that are in error among N total symbols received, the symbol error rate (SER) is calculated as

$$SER = n/N$$

Storage Module

This module is used by the application control in the timed data collection mode. The frequency bin energy information received from the DSP and the current symbol are stored on a 7MB RAM disk configured on the PC (task (xix)). This was necessary to meet the real-time constraint of storing frequency bin energy information at a 4kHz rate. The frequency bin energy values are stored as floating point quantities.

Once all the data for a particular timed test have been stored on the RAM disk, this data is then transferred to hard disk in a certain format (task (xxi)) using compression to save on disk storage, for off-line processing and analysis. On the disk, specific information about the test, as set up by the user in the test configuration, the possible comments etc. are also stored. This puts a particular stamp specific to a test on all collected data. This, it is hoped, would make archiving test data quite convenient.

Access Module

A separate program can be used to access the stored frequency bin information on hard disk. At the present time, the only mode supported is the on-screen display of the symbol, followed by the eight frequency bin energies present in that symbol. This program(RESULTS.EXE under DOS) is not callable from the application control module (or main menu), and has to be called separately from DOS. This routine does the decompression of the stored data on the fly. Typing "DIR DAT" from \NWN directory provides a complete listing of files stored in such a format.

All of the PC software is implemented in Borland C.

TEST MODES

As enumerated in the psuedo-code of the PC software there are four possible test modes. Each of them is described in greater detail in the following subsections.

Waterfall Mode

In the waterfall mode, a real-time display of received characters is available to the user. The host program merely displays the symbols received from the DSP on the user screen as characters. Eighty characters to a line are displayed after which the display of a new line begins. This mode continues indefinitely until interrupted by the user. Because of the overhead required to display symbols on the user screen, only one line of symbols (80) is displayed per second. The remainder of the symbols (4000-80=3200) are not displayed. In this mode, the **baud_offset** variable is also displayed on the upper left-hand corner of the screen. The user can change the value of this variable using the "+" and "-" keys on the keyboard. The PC communicates these key strokes to the DSP board which actually changes the value of the variable and echoes this change back to the PC. Now this changed value of **baud_offset** is used by the DSP in its processing. Using this aid, the user is able to move the window of processing around until a 'decent' scroll of symbols appears on the screen.

Receiver Tuning Mode

The value of baud_offset may also be similarly changed using the "+" and "-" keys in the receiver tuning mode. However, in this mode a real-time display of the symbol error rate, frame slips and bad symbols is displayed on the screen for the user's benefit. The value of **baud_offset** if of course also displayed. Here, the user is able to move the window of processing around until the symbol error rate, frame slips and bad symbols reach a desired value. This is essential before any timed tests performed are considered meaningful. Note that once the value of **baud_offset** is adjusted, and the user does not quit the user interface, this **baud_offset** value remains the same for the remainder of tests as explained earlier. Thus the user can first tune the receiver using either of the two mentioned modes (waterfall or receiver tuning), and then perform any actual symbol error rate tests and/or timed data collection. Eventually this tuning mechanism will be automatic and transparent to the user and probably performed entirely within the DSP.

Symbol Error Rate Mode

This mode is a subset of the Receiver Tuning mode where only the symbol error rate, frame slips and bad symbols are displayed for the user's benefit. The user does not have the capability of changing the **baud_offset** value. This mode is best used after the receiver has been tuned and the **baud_offset** value has been set to the correct value. Then the user is in a position to let the receiver run for any desired length of time and determine what the performance is.

Timed-data Collection Mode

In timed data collection mode, the user has the ability to store symbols, and the energies present in each of those symbols for off-line analysis. Three time levels are supported : 5, 10 and 30 seconds. Again this mode is best used only after the receiver has been tuned. In this mode, the user is only made aware of what the PC host program is doing (collecting data or storing data). Symbols received and the frequency bin energy information of that symbol are stored in RAM first (in real-time) and then stored to the hard disk (in non real-time). This is necessary to meet real-time constraints of the 4kHz symbol rate. No other information about the test is available to the user in this mode. This mode is well suited to performing off-line analysis on the energy present in the various frequency bins in the received symbols. Another useful feature in this mode is that the file associated with each test is user configurable. A set of comments about a certain test may also be incorporated in the stored file, thus providing the user some reference points while accessing that data later for analysis. Compression is used while storing these files to maximize use of disk space. The filenames reflect the configuration parameters associated with a certain test making the files easily identifiable. Each filename label is of the type "Txx-yy-z.NWN", where :

xx = location of test
yy = test I.D.
z = repetition number of test

To access these files later, a separate utility RESULTS.EXE under DOS is available as described earlier. This utility can provide an ascii output of the information in the files, which the user than might use to analyze the received data further.

TAB D

Appendix D

Field Strength Measurements Using GPS System for Site Identification

INTRODUCTION

A series of field strength measurements were performed in coverage areas of the two Oxford, Mississippi, transmitters as a part of Mtel's NWN experiments. A diagram of the setup is provided in Fig. D-1. This report describes the instruments, the setup and cabling details, and the measurement procedure. The experimental setup includes an Anritsu receiver for the field strength measurements, a Trimble Navigation GPS system (Global Positioning System) to identify the location, and a portable PC to control both instruments and to store the data.

ANRITSU RECEIVER

Signal strength was determined by an Anritsu Measuring Receiver MLL 522 B, 300-1000 MHz, battery powered, HPIB equipped with accompanying pig-tail antenna and with a magnetic mount on the roof of the van. At the frequency of 930.9 MHz, the wideband mode (120 KHz) was used to provide a composite field strength over the whole spectrum. The two NWN transmitters use multi-carrier modulation techniques, with four carriers on (present) at any moment, out of eight possible fixed carriers, each 5 KHz apart. The frequency of 930.9 MHz is the center frequency used by MTEL for experimental purposes in development of NWN. The "OL" (Output Level) command has to be sent to the receiver to prompt it to send data back to the PC.

TRIMBLE NAVIGATION GPS SYSTEM

Geographic location was determined by a Trimble Navigation Placer GPS/DR receiver, 10-30 VDC powered, with its own 37-pin connector which provides all other branches needed for a hook-up. The data connector used in this experiment was a 9-pin RS-232 equipped as DTE, using TAIP protocol (Trimble ASCII Interface Protocol). The magnetic mounted antenna was placed on the roof of the vehicle. The gyro-sensor and digital odometer were not connected at this time, and therefore DR (Dead Reckoning) was not used. The receiver uses signals from at least 3 satellites (for data to be valid) to determine its own position. As a default, it

sends a single line of data containing: Universal Time in seconds, latitude, longitude, and the description of data source and validity of data. Data are sent automatically, at approximately 5 second intervals. Therefore, there is no need for a CP (Compact Position) command in the program, which corresponds to this data format, to be sent from the PC.

NATIONAL INSTRUMENTS RS-232/GPIB CONVERTER

Connection of the GPIB equipped Anritsu receiver to the RS-232 port of the PC was accomplished by a National Instruments GPIB-232 CV converter, 9 VDC powered, GPIB and 25-pin RS-232 equipped. This is an IEEE-488 to RS-232, two-way converter. It has two sets of dip-switches which control the mode and transmission parameters of the converter. It was set in a C (controller) mode to control the GPIB equipped Anritsu receiver via the GPIB connector cable. Commands from PC were received by the converter, via the RS-232 port, translated and sent to Anritsu receiver, via the GPIB bus. The receiver response was sent by the Anritsu to the converter via the GPIB bus, translated and sent to the PC via its RS-232 port. The transmission parameters for RS-232 connections were 4800 bits/s, 8 bits, 1 stop bit, no parity.

PERSONAL COMPUTER AS A CONTROLLER

The central controller and data collector was a 4DX33 notebook PC by Compudyne, a 486/33 MHz machine, with a 120 MB hard disk, and only one serial port (9M - pin RS-232). The single serial port controlled two instruments through custom made cabling and some electronics for the proper functioning of both instruments, as well as for uninterrupted storage of data coming from both instruments.

OPERATION

Commands from the PC were received by the converter, via its RS-232 port, translated and sent to the Anritsu receiver via the GPIB bus. The receiver response returned through the same path, traversed in reverse order.

CABLING

Fig. D-2 shows the detailed RS-232 wiring diagram. A source of 9 volts DC was found inside the converter and wired to the unused pin 13 of its 25-pin RS-232 connector. Through the 10K resistor this voltage reversely polarizes the diodes and keeps pin 2 on the 9-pin RS-232 connector on the PC high when no data comes from the instruments. The appearance of data on any one of the two instruments makes the corresponding diode conducting and the voltage drop through the resistor brings data to the PC's pin 2. Hence, the software has to provide that the two instruments send their data alternatively.

PROCEDURE AND A CONTROL PROGRAM

The controlling program was written in Q-BASIC. It asks for typed input of "Anritsu time" (total time for desired field strength measurements), and "GPS time". It was found experimentally that the time allotted to the GPS can be at most 4.5 seconds, if we are to avoid interference with GPS incoming data. The GPS signal comes in at about 5 seconds intervals and is a trapped event on COM1 of the PC. Once the GPS message is received and recorded, control is transferred to the receiver (PC sends OL request to Anritsu), and it starts sending its output level data. If 4.5 seconds is the interval entered, the receiver makes about 18-19 field strength measurements, which are averaged, and only the average value is recorded in the data file. Thus, the data file contains alternate blocks of data, first a GPS block, then an Anritsu block, and so on, until the total time (Anritsu time) has expired, or until F1 is pressed by the operator. The name of the output file is GPSANR.DAT. Table D-1 is an example of the data recorded. The first two columns present the latitude and longitude of the measurement, the "4" is a control character and the rightmost column contains the measured signal strength.

EXPERIMENTAL SETUP

The block diagram is given in Fig. D-1

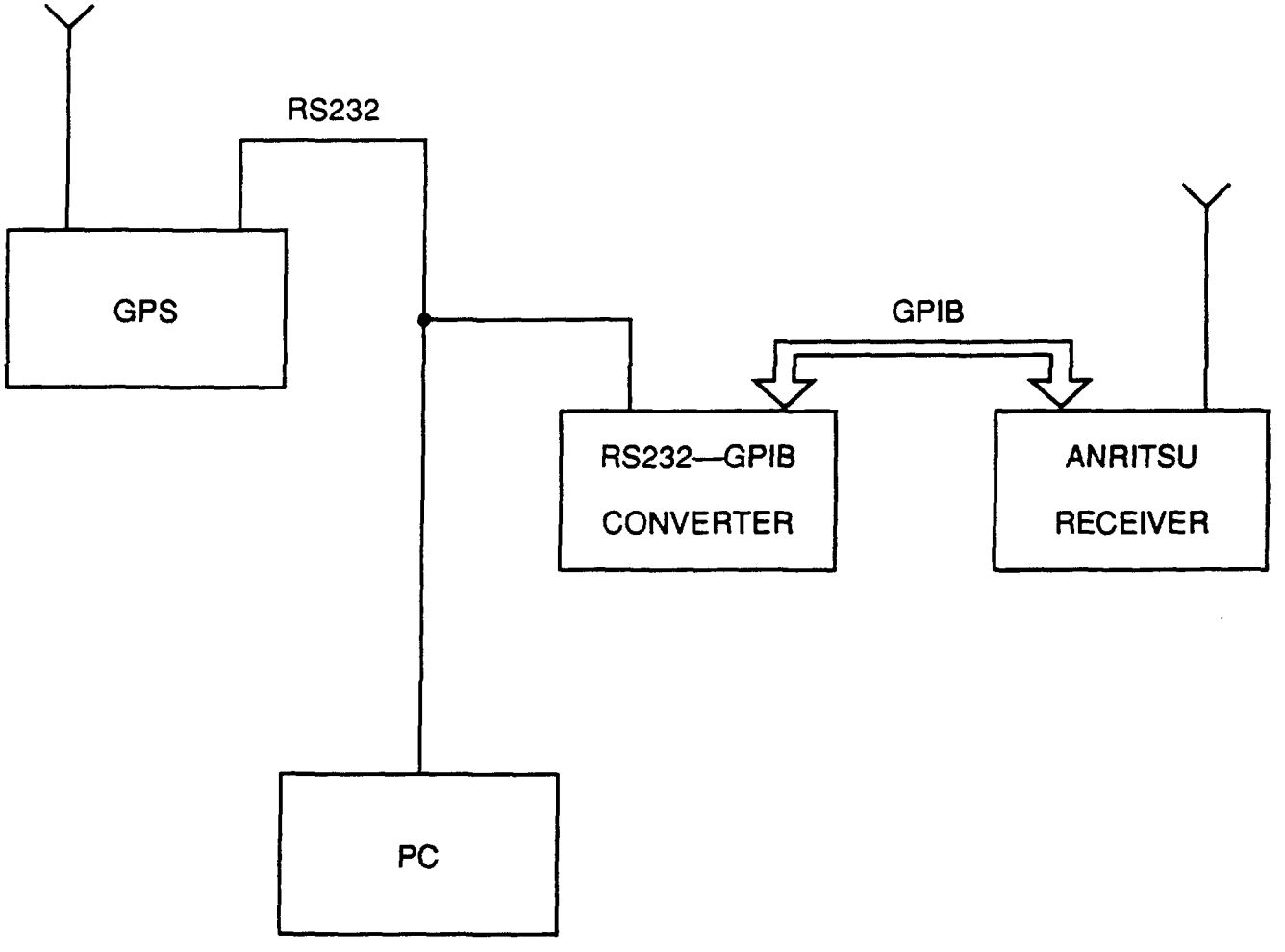

Fig. D-2 depicts the detailed RS232 wiring diagram.

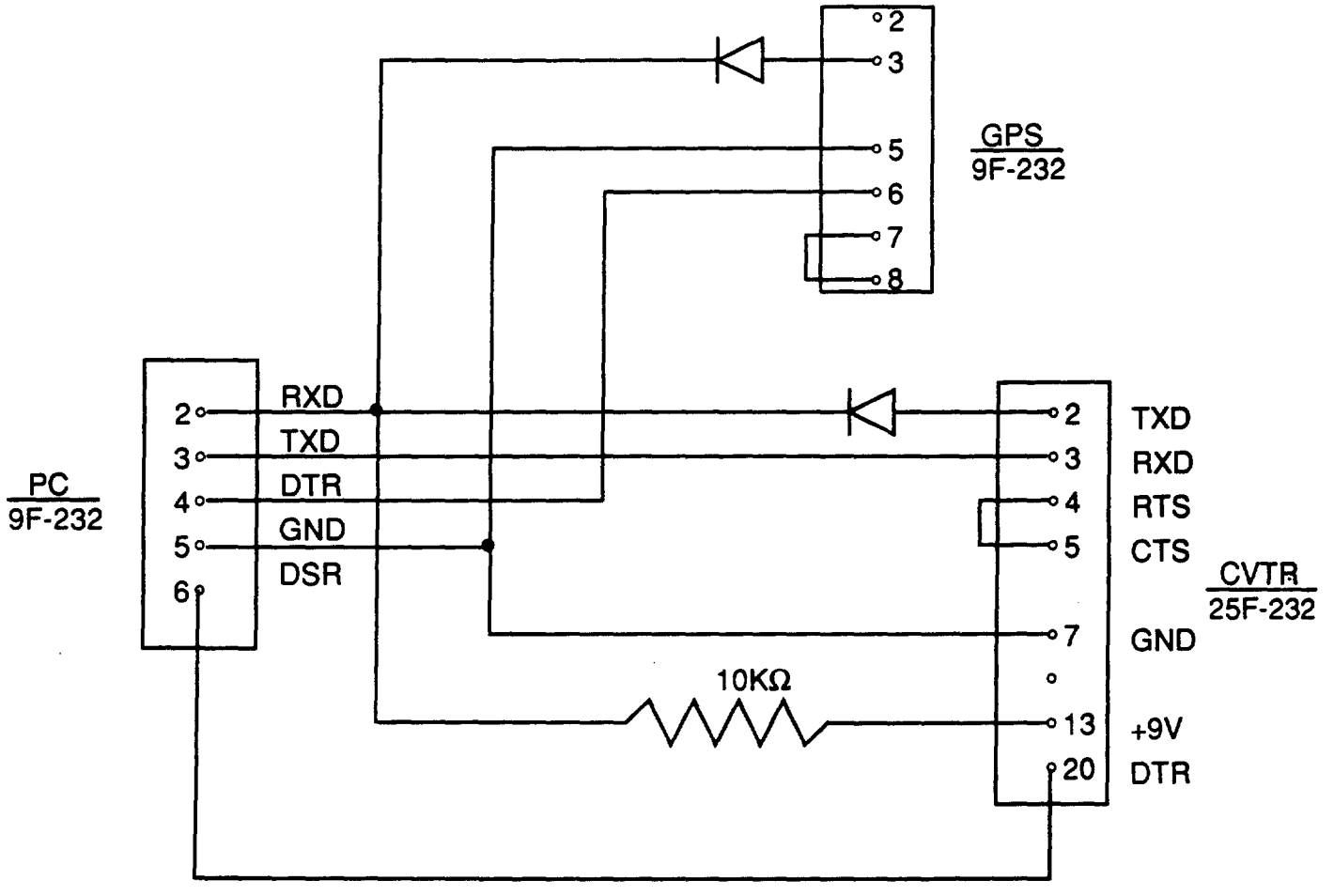

Table D-1

Example of Data Recorded

```
-89.608,  34.3596,4,30.03
-89.61,   34.3595,4,20.42
-89.611,  34.3594,4,15.89
-89.612,  34.3593,4,18.15
-89.614,  34.3592,4,30.68
-89.616,  34.3591,4,37.98
-89.617,  34.359, 4,38.75
-89.618,  34.3589,4,25.75
-89.618,  34.3589,4,18.51
-89.621,  34.3587,4,21.03
-89.621,  34.3586,4,17.53
-89.623,  34.3585,4,28.18
-89.623,  34.3585,4,24.68
-89.623,  34.3585,4,15.76
-89.627,  34.3578,4,25.14
-89.627,  34.358,  4,16.88
-89.63,   34.3576,4,13.21
-89.631,  34.3579,4,13.41
-89.632,  34.3577,4,18.35
-89.632,  34.3577,4,13.11
-89.635,  34.3575,4,17.80
-89.636,  34.3574,4,15.96
-89.638,  34.3572,4,13.06
-89.639,  34.3571,4,9.872
-89.641,  34.357,  4,16.27
-89.642,  34.3569,4,19.82
-89.644,  34.3567,4,24.44
-89.645,  34.3566,4,30.20
-89.646,  34.3564,4,25.65
-89.647,  34.3564,4,14.3
-89.649,  34.3562,4,11.67
-89.65,   34.3561,4,11.24
-89.652,  34.3559,4,8.711
-89.653,  34.3558,4,8.711
-89.655,  34.3557,4,9.605
-89.656,  34.3555,4,10.37
-89.657,  34.3554,4,10.00
-89.659,  34.3552,4,11.8
-89.66,   34.3551,4,15.06
-89.662,  34.355,  4,18.48
-89.663,  34.3549,4,25.98
-89.663,  34.3549,4,25.81
-89.666,  34.3546,4,17.47
-89.668,  34.3544,4,13.53
-89.669,  34.3543,4,15.67
-89.67,   34.3542,4,11.76
-89.67,   34.3542,4,14.9
-89.673,  34.3538,4,12.1
-89.673,  34.3539,4,14.57
-89.676,  34.3536,4,16.33
-89.678,  34.3535,4,17.85
-89.679,  34.3533,4,27.20
-89.681,  34.3532,4,34.56
-89.682,  34.3531,4,35.07
-89.682,  34.3531,4,29.71
-89.685,  34.3528,4,19.98
-89.686,  34.3528,4,14.04
-89.688,  34.3527,4,13.39
-89.689,  34.3527,4,14.15
-89.689,  34.3528,4,10.23
-89.689,  34.3528,4,11.08
-89.689,  34.3528,4,11.57
-89.694,  34.3531,4,11.83
-89.696,  34.3532,4,11.08
-89.697,  34.3533,4,10.54
-89.697,  34.3533,4,8.361
```

TAB E

Appendix E

NWN Testing Program - Fall 1992

The PFSK Transmitter and the PFSK Receiver were brought together during November and December 1992 for testing in and around the Center for Telecommunications in Oxford Mississippi. Details of those test procedures and the results obtained are contained in this Appendix.

The overall System Configuration is shown in Fig. E-1. There are four major subsystems: the clock generation and distribution subsystem; the data generation subsystem; the composite transmitter subsystems; and the receiver subsystem. The design of the transmitters and the receiver are described in separate Appendices; their integration into the system is described here. The other two subsystems, and their role, are also covered in this Appendix.

The starting point, at the upper left of Fig. E-1, is the 2 kHz clock that is input to the analog modulation port of the FM link transmitter. This 2 kHz signal is the "drum beat" which all of the other subsystems use for synchronization. The output of each receiver of this FM signal is connected to the input of a clock sync block that regenerates a 4 kilobaud clock signal and detects the arrival of a multiplexed RESET signal. All of these components merely provide the infrastructure for the core of the experimental system: the transmitters (TX1 and TX2, with their associated data generators) and the receiver, which is found at the lower right of Fig. E-1.

The organization of the remainder of this Appendix follows the

physical flow of the signals. Therefore, in the following section the clock generation and distribution system is described. The following section, "Data Generation and Simulcast Operation" takes up the simulcast operation of the composite transmitters, with particular emphasis on the data generation arrangements. The next section (which forms the bulk of this Appendix) covers the characterization of the receiver itself, using laboratory signal generators. Then, the results of using the receiver to demodulate the signals from the composite transmitters are presented in the section entitled "System Tests". Finally, the "Conclusions and Future Efforts" is given in a brief wrap-up section.

BAUD CLOCK GENERATION, DISTRIBUTION, AND REGENERATION

To surmount the bandwidth limitations of the standard control link that was the connection between the two composite transmitters, Mtel used the control link to distribute a clock signal that had half the speed of the PFSK baud clock. The arrangement of these components is shown in Fig. E-2. A "standard" simulcast system operates at or below 2,400 baud; for these experiments Mtel was sending 24,000 bits per second of data using a 4,000 baud signal. Typical paging industry practice would have the control link distribute the data; clearly, that would not work for these experiments. Indeed, the control link could not even carry the baud clock. Distribution of a half speed clock signal, and insertion of a phase lock loop at each receiver to double the

frequency of that signal, was Mtel's solution. Identical data generators at each composite transmitter were driven by this locally generated baud clock. Synchronization of the data generators was accomplished by multiplexing a RESET signal onto the distributed half speed clock signal. In this manner Mtel could achieve simulcast operation of transmitters without actually broadcasting a 24 kbaud signal on the control link.[1]

The clock source ("2KHZ Gen") was a DYNASCAN 3020 function generator producing a 2 kHz square wave. The pattern synchronization was achieved by a synchronization pulse which could be inserted into clock stream manually or automatically with a variable repetition rate. The pulse insertion is equivalent to bridging the interval between two pulses of the basic clock signal, as is shown on the upper trace in Fig. E-3. The bottom trace shows the signal received in link receivers. Despite evident distortion, which is attributed to the voice channel filters, reliable signal regeneration was achieved.

The regenerated square wave signal is, at the Abbeville location, directly wired to data generator while in the other path (Anderson) a variable delay line is inserted. The purpose of this delay line is to enable investigation of the effects of timing mismatch in simulcast overlap areas. The delay line is implemented by feeding the clock signal, with the inserted RESET pulses,

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[1] The base station transmitters were however transmitting at a 24 kbps data rate.

through a shift register delay line with i stages, where each stage is equivalent to a delay of 32 microseconds. The phase locked loop (PLL) extracts the clock frequency and its phase, but also provides various multiplies of the basic 2 kHz clock. The double frequency is used for baud clock, and 32 kHz is used for the shift register clock. The inserted RESET pulse detection circuit resets the up counter. The counter changes addresses at EPROM address inputs at the leading edge of the 4 kHz pulses coming from the PLL.

DATA GENERATION

The data patterns used for testing are predefined sequences of symbols stored in EPROM circuits. Each byte of data from the EPROM corresponds to a codeword used to assign frequencies to all sub-transmitters according to the composite control line design (see Appendix B). The design of the data generator is presented by the block diagram in Fig. E-4. Using a counter clocked at 4 kHz to address EPROM data locations, the EPROM is cycled through its contents. By hardwiring the higher address lines to high or low voltages the cycle can be limited to subsections of the entire sequence stored in EPROM. In one field test only the lowest 6 address lines were wired to the counter while others were hard wired to the ground so that EPROM constantly cycled through the lowest 64 bytes, which contained each of the 64 distinct symbols in the code table. In another case, 9 address lines were used to obtain a 512 symbols long message. The data lines from EPROM are

latched at the trailing edges of the 4 kHz clock pulses, and forwarded to the transmitter.

SIMULCAST OPERATION OF THE TRANSMITTERS

The testing was performed with two composite transmitters constructed by Glenayre, which are described in Appendix B. One transmitter was located in Anderson Hall, University of Mississippi, and the other was seven miles away, at the Lookout Tower near Abbeville. The arrangement of the clock, data (Message GEN), and composite transmitter subsystems is shown in Fig. E-6. The output from each sub-transmitter output was approximately 5 W, (total power from 4 sub-transmitters of 20 watts) so that the expected signal level in equi-signal areas was -90 dBm or less.

This prediction was experimentally verified in the following manner. The first transmitter was tuned to transmit only the highest and lowest frequency in the channel, while the other was transmitting random data. These two patterns can be distinguished by a spectrum analyzer, as in Fig. E-6, where transmitter 1 dominates, but the signal from transmitter 2 is also above noise. Figures E-7, and E-8 were obtained at the same location a couple inches away, showing nearly equal signals from both transmitters.

RECEIVER TESTING

The receiver was tested in the laboratory environment using an HP 5245A Universal Source (waveform synthesizer). A string of up

to 16 symbols was synthesized in the frequency range below 100 kHz, the baseband range of the receiver. The string was repeatedly generated with no idles in between. Care was taken to avoid any phase shift between symbols, which would broaden signal spectrum. Also, by a suitable choice of symbols in the sequence, in relation to the frequencies of the subcarriers, smooth phase transition between repeated sequences was achieved.

The synthesized waveform is obtained by 12 bit D/A conversion, followed by 100 kHz low pass filter. The sample string Sn, n = 0, 1, 2,..., 2047, was defined as follows:

$$\Phi_{k,0}=0 \qquad k=1,2,3,4$$

$$\Psi_{k,n}=\Psi_{k,n-1}+2\pi\tau f_{k,i}$$

where mk,0 = 0 , k = 1, 2, 3, 4

where mk,0 = 0 , k = 1, 2, 3, 4

where $f_{k,i}$ is the frequency of kth subcarrier (k = 1,2,3,4) during ith symbol interval (i = 1,2,..., I).

g is the time interval between samples:

g = I/(2048*R)

where R is the symbol rate.

In one example Mtel used I = 16, R = 4000 baud, g = 1.95 microseconds, and the frequencies of the subcarriers were chosen from the set (40 kHz, 45 kHz, 50 kHz, 55 kHz, 60 kHz, 70 kHz, 75

kHz). Figure E-9 shows a typical 200 microsecond window of a test signal. The upper trace shows the time domain sample, the middle left trace shows the spectrum obtained by FFT processing in the range (0 - 5 MHz), while the bottom trace shows the spectrum in the range (0 - 100 kHz) with 5 kHz resolution. It is obvious that the symbol contains four subcarriers at 45 kHz, 55 kHz, 65 kHz, and 75 kHz which corresponds to the +SYNC symbol.

In order to avoid abrupt changes of the phase at the symbol sequence restart, the symbol set is chosen so that each frequency has integer number of periods in the whole sequence. For example, a 55 kHz subcarrier, during one symbol that is 250 microseconds long, completes 13.75 periods. It takes four symbols containing the 55 kHz subcarrier (not necessarily consecutive) in the sequence, to provide an integer number of periods. In this way spectrum broadening due to phase shifts is avoided. Fig. E-10 shows spectrum of a typical 16 symbol sequence generated for the test purposes.

The test signal obtained from HP 5245A universal source can be connected directly to the A/D converter of the receiver, as shown in Fig. E-11, for digital section testing. External clock was provided for synchronization of the baud interval and the FFT window. With this setup we have achieved error free detection of symbols for several hours, which is equivalent to a BER < 10 -9. These tests confirmed that real time signal detection using FFT processing is feasible. These tests also provided basic tools for

evaluation of the effects of the additional signal processing necessary in real systems.

The next set of tests were designed to introduce RF processing in the transmitter - receiver path. Block diagram of the test setup is given in Fig. E-12. A baseband test signal from the waveform synthesizer is coupled to the AM modulation input of an HP 8656B signal generator set for 40% AM. The "baseband" frequency of the sub-carriers was in the 30 kHz - 65 kHz region, and the signal generator RF carrier frequency was 930.8525 MHz, so that the upper sideband fits the receiver channel. The carrier and lower sideband play the role of adjacent channel interference. This interference was successfully rejected by receiver filters and error free reception was achieved. This test proved the basic functionality of the RF section of the receiver.

The first step was determination of the dynamic range of the receiver. By varying the signal generator output level and observing the symbol error rate the dynamic range of the receiver can be determined. Too high a signal causes errors due to nonlinear effects, and a signal that is very weak is corrupted by noise. Error free operation was achieved when the input signal was in the range between - 63 dBm and - 112 dBm, i.e., the dynamic range is 49 dB.

Then, the receiver sensitivity to jitter was investigated. In one test the FFT window position was moved relative to the center of the symbol interval. Error free operation was achieved with

deviations of +/- 37.5 microseconds, which corresponds to +/- 15% of a symbol interval. In another test sinusoidal phase jitter was introduced into the clock signal -- error free operation with +/- 31.25 microseconds of jitter was observed. Finally, the symbols were alternately extended and shortened at the source in 1.95 microsecond steps. Error free performance was obtained with +/- 33.15 microseconds of jitter.

The last set of lab tests determined the sensitivity of the system to frequency deviations. The signal spectrum at the A/D converter input, relative to its nominal position, was altered by varying the frequency of a local oscillator in the receiver. Error free operation with frequency deviations of +/- 1100 Hz was observed.

These lab tests characterized the receiver, in isolation, so that in the system tests that followed the additional degradation due to clocking, transmitters, and the propagation path could be identified.

SYSTEM TESTS

In the first part of the field test, the receiver was stationary in the National Center for Physical Acoustics building, nearly one mile from the Anderson Hall transmitter. The signal strength was approximately -80 dBm. The block diagram of the test setup is given in Fig. E-13. Symbol timing information was extracted from the 930.1 MHz channel used for synchronization of

simulcast transmitters. Error free operation for several hours was achieved, which corresponds to a symbol error rate of less than one error in 10^8 symbols.

By inserting an attenuator, the signal level was reduced in order to investigate the receiver sensitivity. Error free operation was observed at average signal levels above - 95 dBm. This apparent loss of sensitivity in comparison to the lab tests is attributed to the time varying fading in field tests and the frequency inaccuracies in some of the sub-transmitters.

The sensitivity to jitter was tested by changing the FFT window position relative to the symbol interval. Within a +/- 28.1 microsecond jitter range error free operation was obtained. This reduction in the tolerance to jitter, in comparison to the lab tests is attributed to:

the long (88 microsecond) transition intervals between symbols in the composite transmitters;

the dynamic frequency errors in several of the sub-transmitters; and

jitter in the clock extraction circuit (PLL).

Nevertheless, the tolerance observed was better than the target of +/- 25 microseconds.

Sensitivity to frequency deviations was checked by varying the frequency of a local oscillator in the receiver. Error free operation was obtained when the signal was within +/- 650 Hz of the nominal frequency. This is a substantial degradation in comparison to the lab tests. It was also observed that the tolerance to

frequency variations depended upon the data pattern. This led to finding that a subset of sub-transmitter frequencies deviated from their nominal values much more in the dynamic regime (when data are transmitted) than they do during static testing. These deviations exceeded 2 kHz in one sub-transmitter. Adjustments of the dynamic deviation brought the frequency deviations down to approximately +/- 400 Hz. This can be, and should be improved for future tests. Nevertheless the tolerance of a DSP receiver to frequency deviations was much higher than had been predicted, which is important for the design of simple receivers.

Further field tests were performed with the receiver in a van, traveling through the coverage area of both transmitters. Error free reception was attained in areas where signals from either transmitter 1 or 2 dominate, as well as in areas where the signals are approximately equal.

CONCLUSION AND FUTURE EFFORTS

The tests of forward channel NWN radio link performed in November and December 1992 have shown that PFSK can provide a 24 kb/s gross bit rate in while staying within the FCC specified 50 kHz channel mask and can operate in a simulcast environment. Reception is error free if the signal strength, jitter, and frequency deviations are within acceptable bounds.

Timing variations of more than 50 microseconds can be tolerated. Further improvements are expected when the transmitter

inter-symbol transitions are reduced from the current 88 microseconds to approximately 50 microseconds.

The receiver was tolerant of frequency aberration. It is estimated that an overall frequency perversion (transmitter plus receiver) of more than 500 Hz can be tolerated, but the uncontrolled transmitter frequency errors must be significantly below this figure before precise quantification of the tolerance can be made.

The dynamic range of the receiver was nearly 50 dB, which was adequate for testing. Additional transmitter tuning is necessary before final receiver sensitivity tests can be completed.

Other system imperfections, such as leakage radiation from sub-transmitters and combiners, intermodulation products at transmitters, and frequency selective fading, were not a cause of problems in the experiments.

Clock extraction from the PFSK signal will be the prime development task in the immediate future.

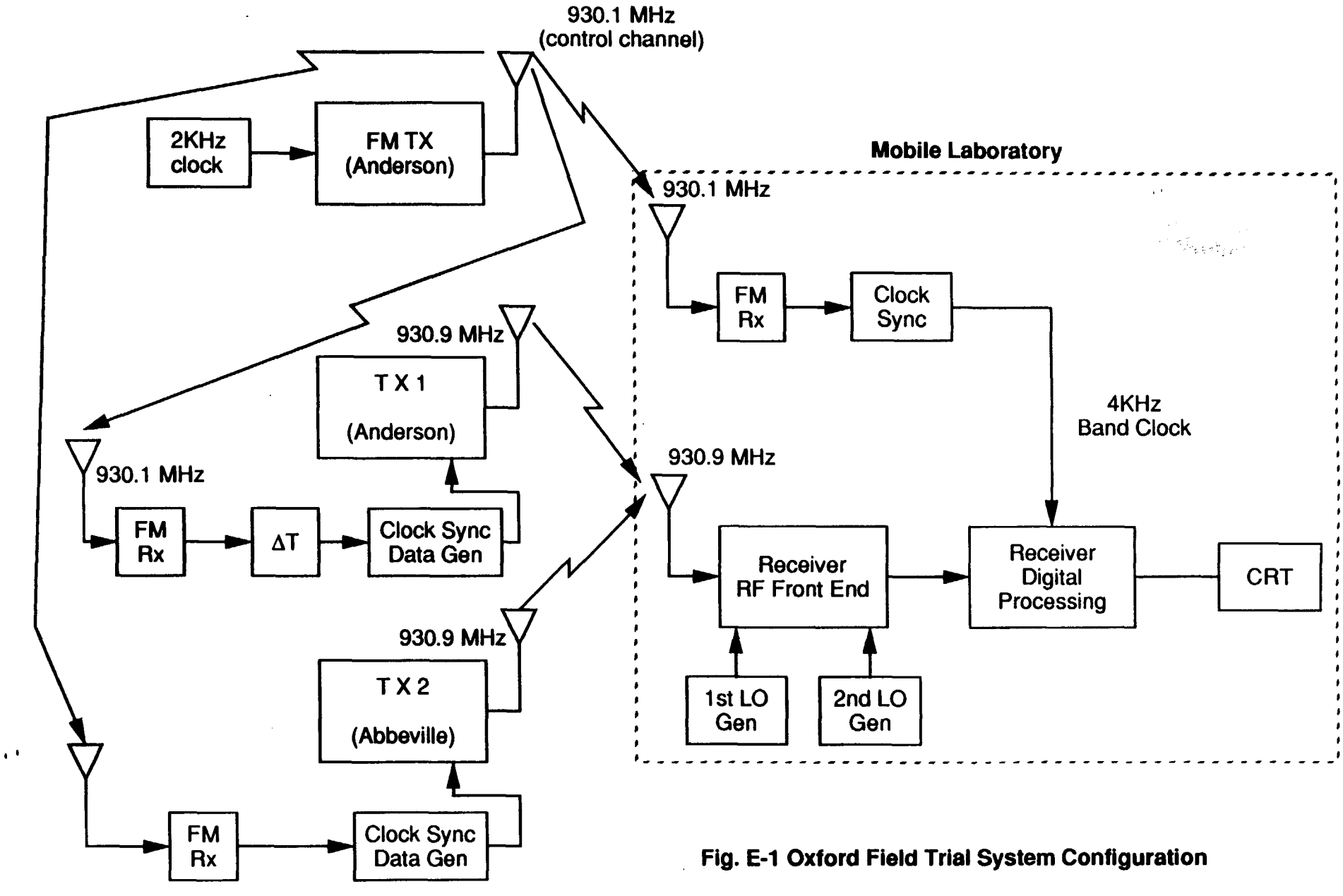

Fig. E-1 Oxford Field Trial System Configuration

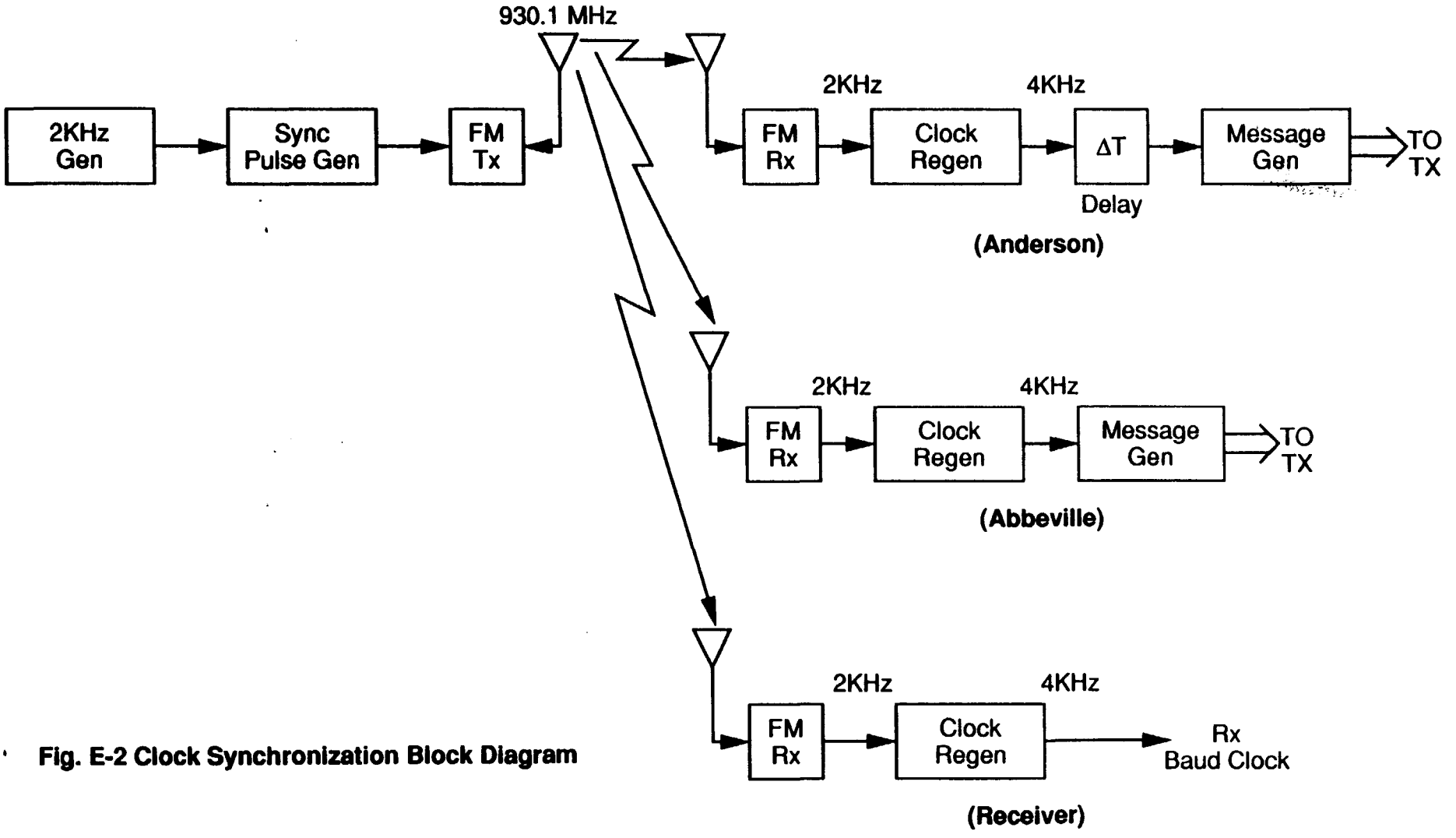

Fig. E-2 Clock Synchronization Block Diagram